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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,492	04/01/2004	Tarek Eldin	X-1481 US	8518

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 09/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,492	ELDIN ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/10/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *17* is/are withdrawn from consideration.

5)☒ Claim(s) *9* is/are allowed.

6)☒ Claim(s) *1-8 and 10-16 & 18-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered July 10, 2006.

- Claims 1-25 are pending. Claims 1, 9, 10, 16, 18-19 & 23 are amended.
- Claim 17 is canceled.
- Claim 9 is allowed.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to amended claims 1, 10, 16, 18-19 & 23 and previously presented claims 2-9, 11-15, 17, 20-22 & 24-25 filed July 10, 2006 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends that; Dastidar does not teach a method of isolating a fault on a line segment of a switch matrix, a connectivity graph is not the same thing as a layout or schematic, Dastidar only generates non-overlapping routes, hence teaching away from claim 6 and Dastidar does not teach a failure analysis software. The examiner respectfully disagrees.

Regarding the contention that Dastidar does not teach fault isolation to the point where specifically pointing out the exact interconnect point and the points adjacent to it, the examiner agrees, and hence claim 9 is allowed. However, the examiner would like to point out that the recitation "a method of isolating a fault" has not been given

patentable weight in the remaining independent claims because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Further given the broadest possible interpretation of claims 16 and 23, it is requested that applicant makes the claims more specific as to fault isolation because although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Further Dastidar teaches the connectivity graph, which as evidenced by the specification can be interpreted as the same thing as a layout: "The connectivity graph contains a map of a programmable integrated circuit. The connectivity graph is a representation of all of the programmable elements on the programmable integrated circuit. The connectivity graph can map programmable connections in the interconnect structure, programmable logic elements, and any other circuit elements. The connectivity graph can include a representation of a hierarchical interconnection structure with global and local conductors. The connectivity graph includes representations of all of the possible programmable states of the programmable circuit elements on the programmable integrated circuit" (column 4, lines 5-20). Further Dastidar does not only generate non-overlapping routes but all Dastidar mentions is

that the routes that are tested at the same time i.e. in the same iteration cannot be overlapping. "A configuration file 113 can include more than one route. All of the routes in one configuration file can be tested at the same time. Routes that are tested at the same time cannot include overlapping circuit elements or overlapping connections. Routes that do not include overlapping elements can be included in one configuration file and tested at the same time" (column 2, lines 59-65). Dastidar clearly mentions that "Ideally, there are enough configuration files to test every possible connection on the PLD. For example, if there is an 8 input, one output multiplexer on a PLD, there should be at least 8 different configuration files to test the connections for each of the 8 inputs. Each configuration file is used to test the connection for one of the multiplexer inputs. Eight test cycles are needed to test an 8 input multiplexer, because overlapping connections cannot be tested at the same time" (columns 2-3, lines 65-7). Lastly, all the test results are fed into the simulator, which then analyses the results, and hence overcomes the limitation of the failure analysis software.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-8, 10, 13-16, 18 & 20-25 are rejected under 35 U.S.C. 102(e) as being unpatentable over Dastidar et al. US Patent no. 7,024,327 B1.

As per claim 1:

Dastidar et al. teaches a method of isolating a fault on a line segment of a switch matrix comprising (columns 1-2, lines 65-2): generating a first route between an input of the switch matrix and an output of the switch matrix through a first programmable interconnect point (Figure 1 # 121, column 2, lines 10-25) on the line segment and through a first adjacent programmable interconnect point (column 3, lines 32-35); configuring the first route in the switch matrix (column 2, lines 25-30); applying a first test vector at the input (column 2, lines 30-35); measuring first test data at the output (column 2, lines 30-35); storing the first test data (Figure 1 # 123, column 3, lines 10-25) and at least a portion of the first route (Figure 1 # 113); generating a second route between the input and the output (column 3, lines 25-30) through the first programmable interconnect point on the line segment and through a second adjacent programmable interconnect point (column 3, lines 32-35), configuring the second route in the switch matrix (column 3, lines 25-30); applying a second test vector at the input (column 3, lines 30-32); measuring second test data at the output (column 3, lines 25-36); and storing the second test data and at least a portion of the second route (column 3, lines

25-35); and evaluating the first test data and the second test data against a layout schematic of a programmable logic device (column 2).

As per claim 2:

Dastidar et al. teaches the method as rejected in claim 1 above, wherein a path from the adjacent programmable interconnect point to one of the input and the output is generated by an auto- route tool (Figure 3, # 302).

As per claim 3:

Dastidar et al. teaches the method as rejected in claim 2 above wherein the path excludes the line segment (column 4, lines 50-60).

As per claim 4:

Dastidar et al. teaches the method as rejected in claim 1 above wherein the first adjacent programmable interconnect point is on the line segment (column 4, lines 46-48).

As per claim 5:

Dastidar et al. teaches the method as rejected in claim 1 wherein the switch matrix is incorporated in a programmable logic device (columns 1-2, lines 65-2).

As per claim 6:

Dastidar et al. teaches the method as rejected in claim 1 wherein the second test vector is the same as the first test vector (column 3, lines 55-65).

As per claim 7:

Dastidar et al. teaches the method as rejected in claim 1 wherein the step of generating the second route is performed prior to the step of applying the first test vector (column 2, lines 20-25).

As per claim 8:

Dastidar et al. teaches the method as rejected in claim 7 above wherein the first route and the second route are stored in a route directory (Figure3 # 303, column 5, lines 10-15).

As per claim 10:

Rejected under the same grounds as claim 1 above.

As per claim 13:

Dastidar et al. teaches the method as rejected in claim 1 above, wherein the line segment includes at least four programmable interconnect points (column 4, lines 46-48).

As per claim 14:

Dastidar et al. teaches a method of isolating a fault on a line segment of a switch matrix comprising: (a) identifying original programmable interconnect points (PIPs') in the line segment (column 4, lines 1-11); (b) looking up adjacent PIPs in a PIPS database, each of the adjacent PIPs being adjacent to at least one original PIP (Figure 3 # 301, column 4, lines 1-11); (c) generating a first route through a first port of the switch matrix to an Nth original PIP where N is an integer (column 4, lines 43-46); (d) adding a second route from the Nth original PIP to an Mth adjacent PIP where M is a second integer (column 3, lines 43-46); (e) adding a third route from the adjacent PIP to

a second port of the switch matrix (column 3, lines 43-60); (f) storing a route including the first route, second route, and third route in a route directory (Figure 1 # 113, column 3, lines 25-35); (g) repeating steps (d), (e) and (f) for all adjacent PIPs adjacent to the original PIP (column 3, lines 25-36); (h) repeating steps (c), (d), (e), (f) and (g) for all original PIPs (column 3, lines 25-36); (i) configuring the route in the switch matrix (column 3, lines 25-30); (j) applying a test vector at an input of the route (column 2, lines 30-35); (k) reading test data at an output of the route (column 6, lines 5-13); (l) storing the test data (Figure 1 # 123, column 3, lines 10-25); and (m) repeating steps (i), (j), (k) and (1) for all routes in the route directory (column 3, lines 25-36).

As per claim 15:

Dastidar et al. teaches a system of isolating a fault on a line segment of a switch matrix comprising: means for identifying original programmable interconnect points on the line segment (column 4, lines 1-11); means for identifying programmable interconnect points adjacent to each of the original programmable interconnect points (Figure 3 # 301, column 4, lines 1-11); means for generating routes between an input of the line segment and an output of the line segment through each of the programmable interconnect points adjacent to each of the original programmable interconnect points (column 4, lines 43-46); and means for testing the routes (column 2, lines 30-35).

As per claim 16:

Dastidar et al. teaches a system for fault isolation on a line segment in an integrated circuit (IC) having at least one programmable interconnection (column 3, lines 32-35), the system comprising: a database having the at least one programmable

interconnection in the IC (column 4, lines 1-11); having a test path generation software module (Figure 3, # 302), the test path generation software module comprising: code for identifying original programmable interconnections on the line segment having a fault (column 4, lines 1-11); code for identifying programmable interconnections adjacent to the original programmable interconnect points (Figure 3 # 301, column 4, lines 1-11); code for generating routes between an input of the line segment and an output of the line segment through the original programmable interconnections and through the programmable interconnections adjacent to the original programmable interconnections (column 4, lines 43-46); and a tester coupled to the processor and the IC having the line segment, the tester for testing the line segment using the generated routes (column 6, lines 5-20), a failure analysis software (simulator).

As per claim 18:

Dastidar et al. teaches the system as rejected in claim 16 above further comprising: a test input file comprising the generated routes and test vectors for the generated routes (Figure 3 # 303), the file sent to the tester by the processor (column 6, lines 1-20); a test results file comprising the test results on the line segment from the tester (column 9, lines 1-20); and a failure analysis module stored in the memory for evaluating contents of the test results file (column 9, lines 1-20).

As per claim 20:

Dastidar et al. teaches the system as rejected above in claim 16 wherein the database further comprises the original programmable interconnections (column 4, lines

1-11) and the programmable interconnections adjacent to the original programmable interconnections (Figure 3 # 301, column 4, lines 1-11).

As per claim 21:

Dastidar et al. teaches the system as rejected above in claim 16 wherein the IC comprises a programmable logic device (PLD) (columns 1-2, lines 65-2).

As per claim 22:

Dastidar et al. teaches the system as rejected above in claim 21 wherein the database further comprises all the original programmable interconnections on the PLD (Figure 3 # 301, column 4, lines 1-11).

As per claim 23:

Dastidar et al. teaches a method for fault isolation on a line segment in an integrated circuit (IC) having at least one programmable interconnection (column 3, lines 32-35), the method comprising: identifying an original programmable interconnection point on the line segment having a fault (column 4, lines 1-11); identifying an output programmable interconnection points adjacent to the original programmable interconnection point (Figure 3 # 301, column 4, lines 1-11); and generating a route between an input of the line segment and an output of the line segment through the original programmable interconnection point and through the output programmable interconnection point (column 4, lines 43-46).

As per claims 24 & 25:

Claims 24 & 25 are directed to a method of the system of Claims 16-22. Dastidar et al. teaches as stated above, the system as set forth in Claims 16-22. Therefore, Dastidar et al. also teaches as stated above, the method as set forth in claims 24 & 25.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11, 12, & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dastidar et al. US Patent no. 7,024,327 B1.

As per claims 11 & 12:

Dastidar et al. teaches the method as rejected in claim 10.

Dastidar et al. does not explicitly teach a method wherein there are' at least three first digital test values in the first series and there are at least three second digital test values in the second series.

However, it would have been obvious to one of ordinary skill in the art to have at least three digital test values in the first and second test series, since one of ordinary skill in the art would have recognized that Dastidar et al. is already using functional digital test data vectors to test the device (column 6, lines 1-20). These functional test vectors include test vectors, expected results and test values; hence it would be obvious to represent them with three different digital test values. In addition it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum range or workable range involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 19:

Dastidar et al. teaches the system as rejected above in claim 18.

Dastidar et al. does not explicitly teach the system wherein information used by the tester from the test input file is modified based on feedback from the failure analysis module.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the test input file based on feedback from the failure analysis module because one of ordinary skill in the art would have realized that doing so would enable Dastidar et al.'s invention to cross check for a diverse number of errors. Further it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum range or workable range involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

The present invention pertains to a circuit and method for testing programmable interconnecting points of the Field Programmable Gate Arrays (FPGA).

The claimed invention recites features such as: "a method of isolating a fault on a line segment of a switch matrix comprising: generating a first route between an input of the switch matrix and an output of the switch matrix through a first programmable interconnect point on the line segment and through a first adjacent programmable interconnect point; configuring the first route in the switch matrix; applying a first test vector at the input; measuring first test data at the output; storing the first test data and at least a portion of the first route; generating a second route between the input and the output through the first programmable interconnect point on the line segment and through a second adjacent programmable interconnect point, configuring the second route in the switch matrix; applying a second test vector at the input; measuring second test data at the output; and comparing the first test data and the second test data against a layout schematic of a programmable logic device so as to locate the fault on the failed line segment" (claim 9).

The prior art of record Dastidar et al. US Patent no. 7,024,327 B1, teaches generating routes and performing a series of tests to detect the presence of any manufacturing detects. Merely detecting the defect occurs along a line segment somewhere along that path. Dastidar et al. does not anticipate or render obvious isolating the specific programmable point, where the defect occurs.

The prior arts of record fail to anticipate or render obvious the present invention. Therefore claim 9 is allowable over the prior arts of record.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. (6694464 B1, 6470485 B1, and 6725442 B1) mention the same interconnection testing system wherein test vectors are scanned after generating routes.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S.S

Saqib Siddiqui
Art Unit 2138
08/31/2006

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